Deep Dive – M-CRPS Input Impedance Test Procedure Using a Venable FRA

The following covers key questions shared by a Venable customer after reviewing Michael Gray's recent blog post M-CRPS Input Impedance Test Procedure Using a Venable FRA

1. *Is the recommended test method in the MCRPS spec misleading or incomplete? In your example, the reported impedance at 184Hz is actually capacitive. Also you ask which of the inductances is correct/should be reported.*

What caught my attention when reviewing the M-CRPS specification was the PSU Input Impedance-Phase Figure L-2 plot below:

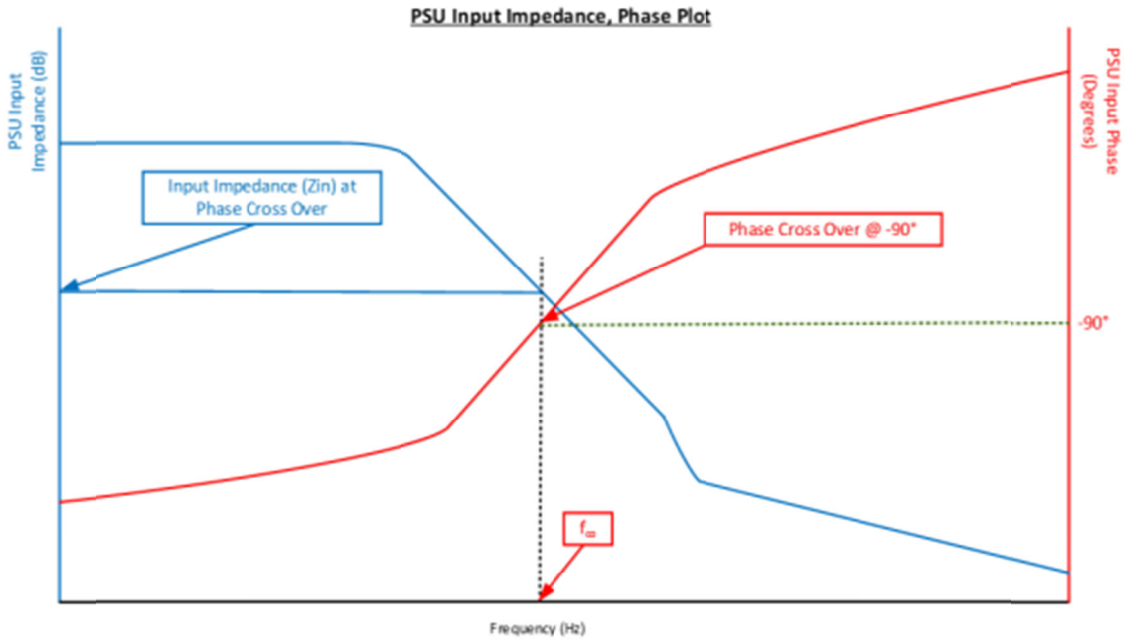
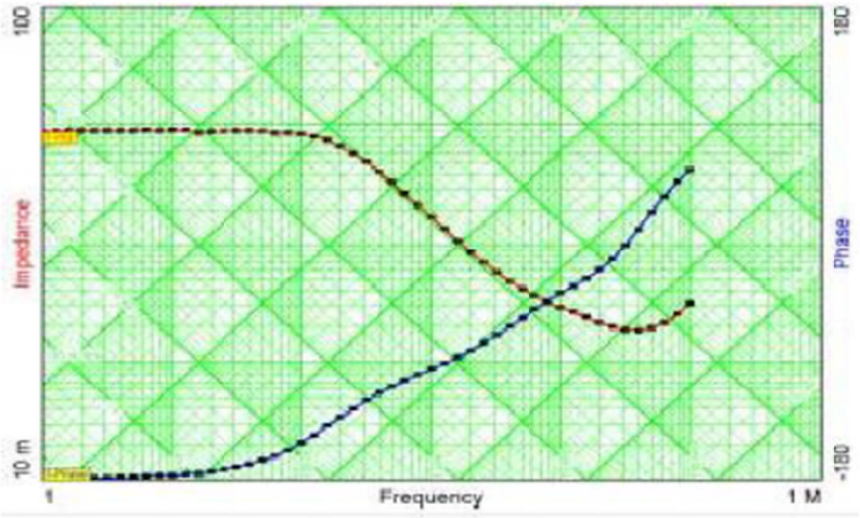


Figure L-2. Sample Impedance / Phase Plot

I compared this sample plot with actual DC-DC converter input impedance plots I have measured and the response is fairly typical. The low frequency input impedance is a negative resistance which becomes capacitive as the amplitude rolls off at higher frequencies. It eventually becomes resistive and then inductive at even higher frequencies.



According to Figure L-2, the inductance is calculated from the impedance where the phase crosses -90 degrees. However, this point is actually capacitive. A capacitive reactance has a phase -90 degrees and the amplitude response rolls off as the frequency increases. Could this be a negative inductance that is being measured? You would not be able to tell the difference between a capacitor or a negative inductor measuring a single point frequency point. You have to look at the complete response. At -90 degrees, in this plot, the response falls off as function of increasing frequency as a capacitor would. A negative inductance will have the same increasing amplitude response with respect to increasing frequency as a positive inductance but the phase would be shifted by 180 degrees to -90 degrees.

I'm not sure what the purpose of having a minimum inductance specification Lin of 11mH/kW (See section 5.1.17 and section 5.3.3) but the methodology used in Supplemental Material O. that is used to calculate it is incorrect. For whatever reason, this specification doesn't apply to the Low Voltage +54 VDC rack power (See section 5.2).

2. *What other improvement do you strongly believe should be part of this test method?*

I think the Input Impedance Measurement setup Supplemental Material O. of using an NMOS in series with the input to Inject a disturbance is a very inefficient. A high saturation current transformer with an amplifier would work better when injecting a voltage in series. The current injection method would work the best with minimal cost.

3. *Do you have any concerns of using the current injection method instead? I think it is a good idea to also document this as an alternative test method from what is already presented.*

I think it would good idea to add the current injection method to the document as an alternative injection method. I think of the current injection as modulating a load However, there is no turnkey method for doing this type of measurement. Some commercial electronic loads have this capability but are limited by higher frequency bandwidth. Most people build their own because of voltage current or power needs.

