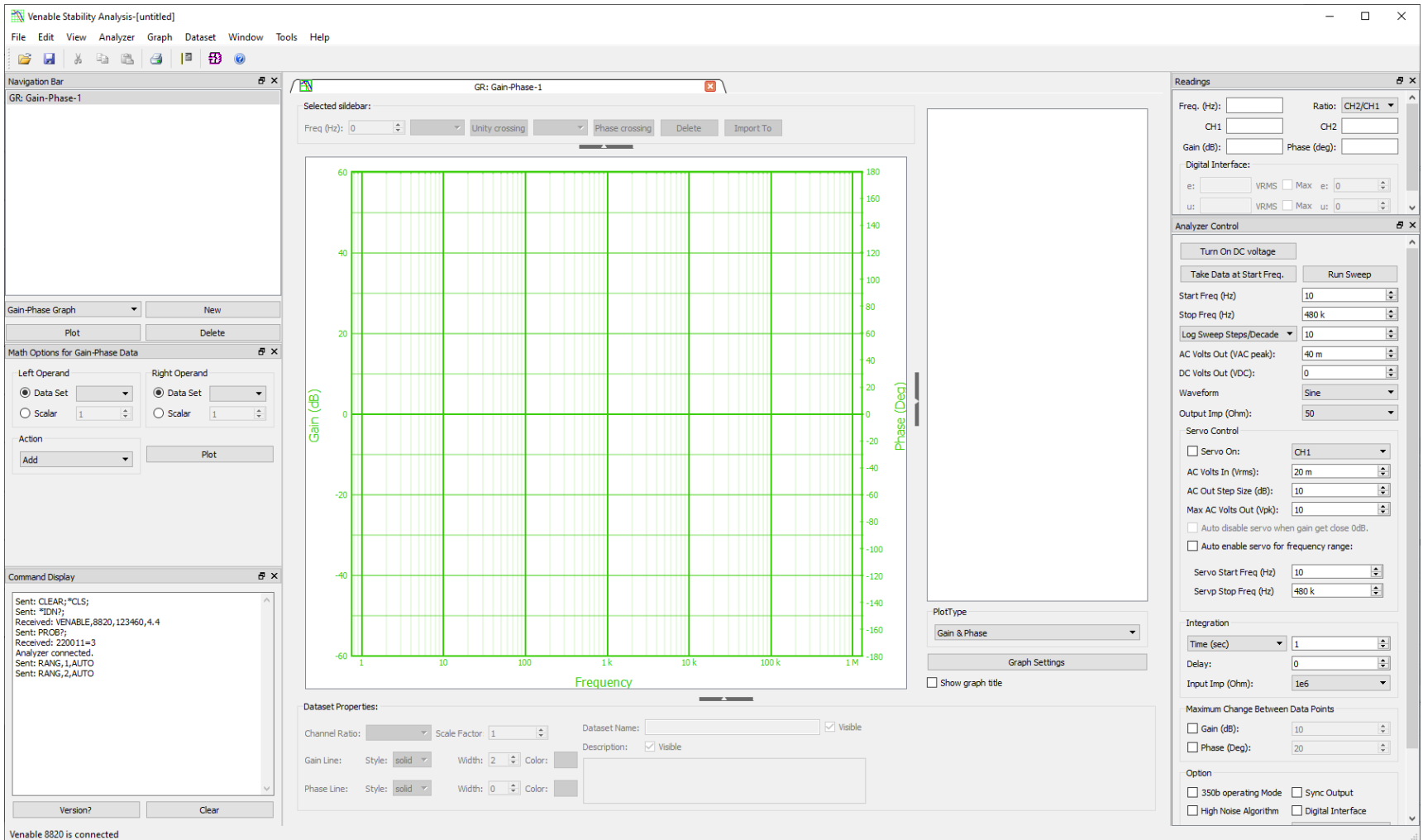




Venable Instruments Training Session

Stabilizing Power Supply Control Loops

Venable 7.0 Stability Analysis Software



Version 7 Stability Analysis Software

- Python based: platform independent and fewer lines of code
- Docking windows and tabbed structure
- Multiple graphs with multiple plots can be saved in one file
- Software uses Windows[®] USB driver
- Plug and play with easy connection to the analyzer
- Compatible with Windows[®] 7, 8, 8.1, 10 and 11

Venable 7440



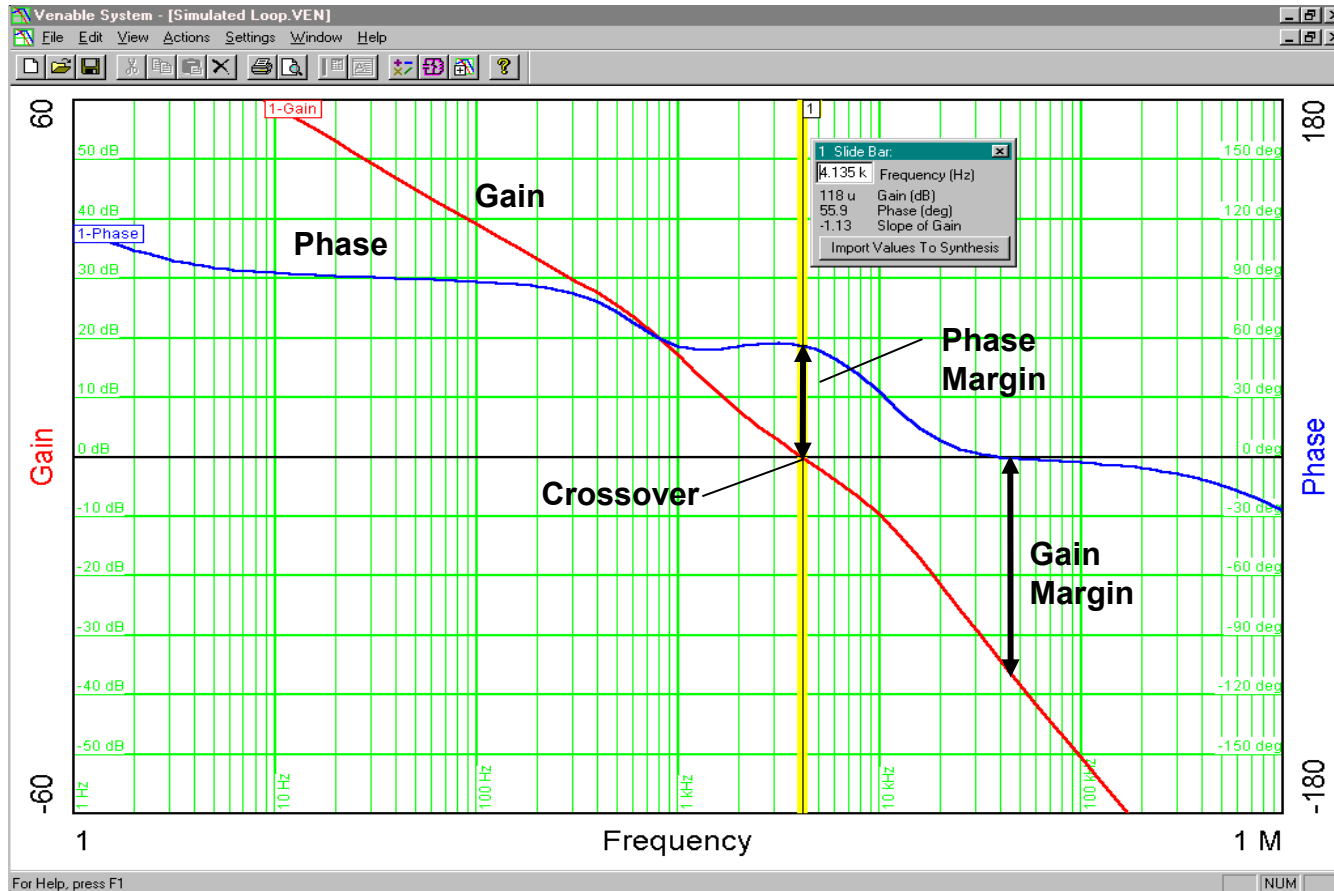
Specifications

- 10 μ Hz to 5/20/40 MHz
- 2, 3, or 4 Input channels
- 10mVpk-500Vpk input range
- Generator and channels isolated to 600 Vpk
- Can measure absolute phase referred to the generator
- IEEE 488 and USB 2.0 are standard interfaces

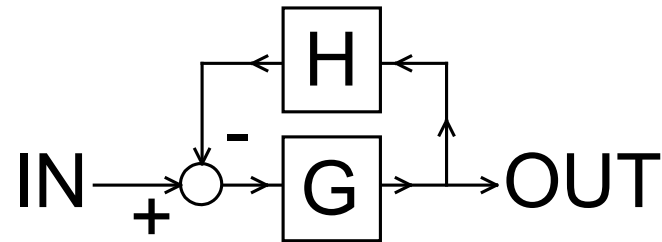
Loop Gain Measurements

- Stability Criteria
- Loop Gain Measurements
- Stabilizing Feedback Loops

Closed Loop Circuit Bode Plot of Loop Gain



A LITTLE BIT ABOUT SIGNALS

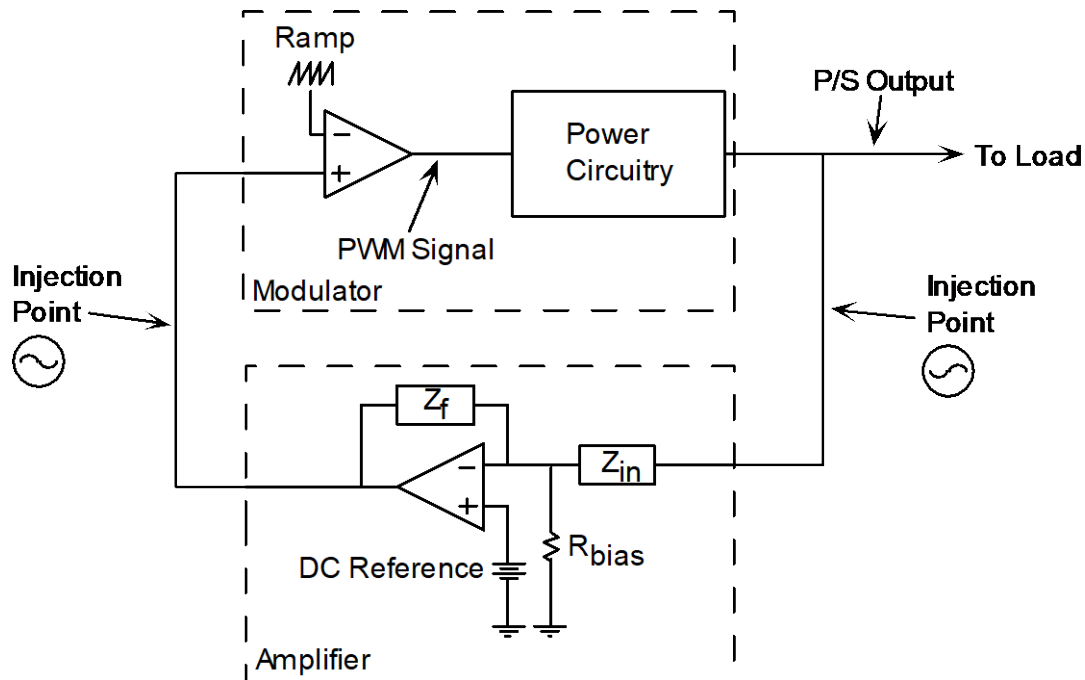


$$G \quad a = \frac{G}{1+G}$$

$$G \quad a = \frac{1}{H} \times \frac{G}{1+G} \times H$$

Loop gain is not GH. Loop gain is -GH.

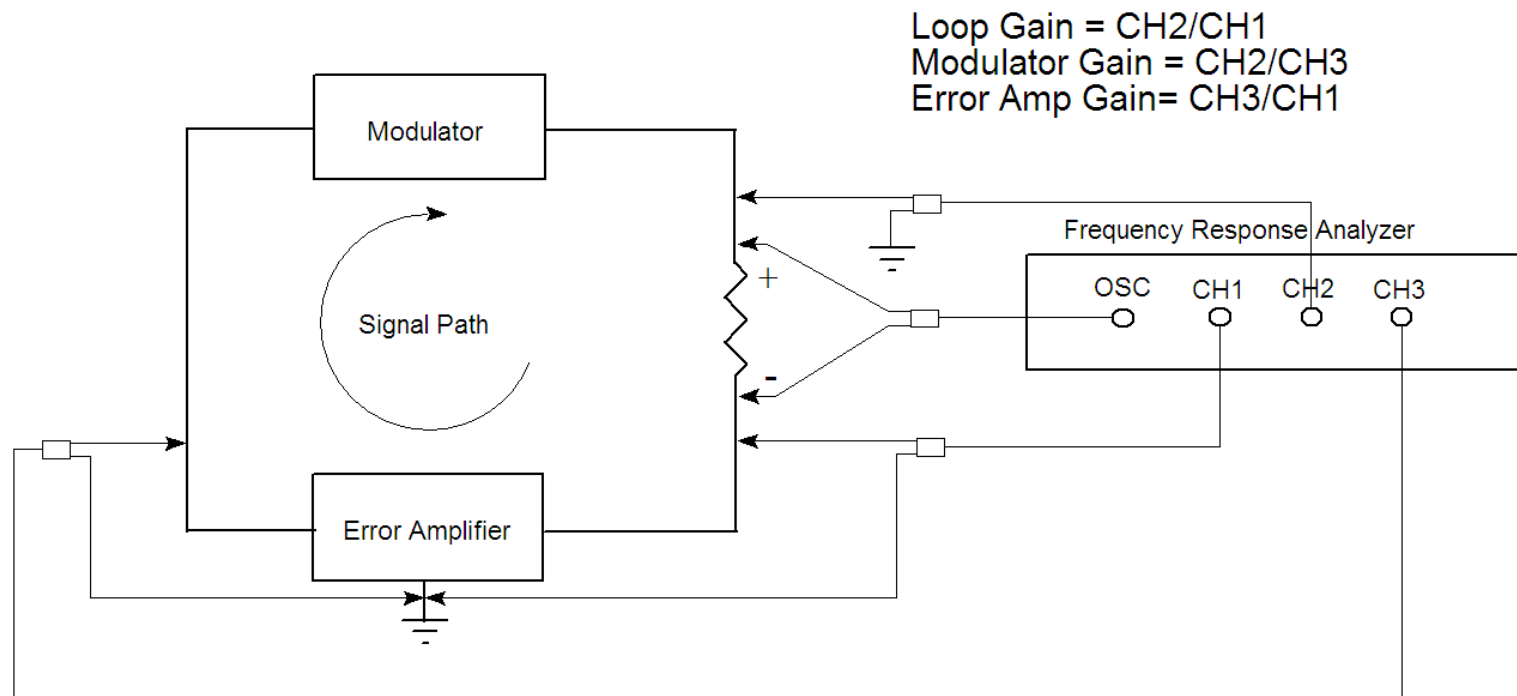
Closed Loop Circuit



Measuring Loop Gain with the Loop Closed

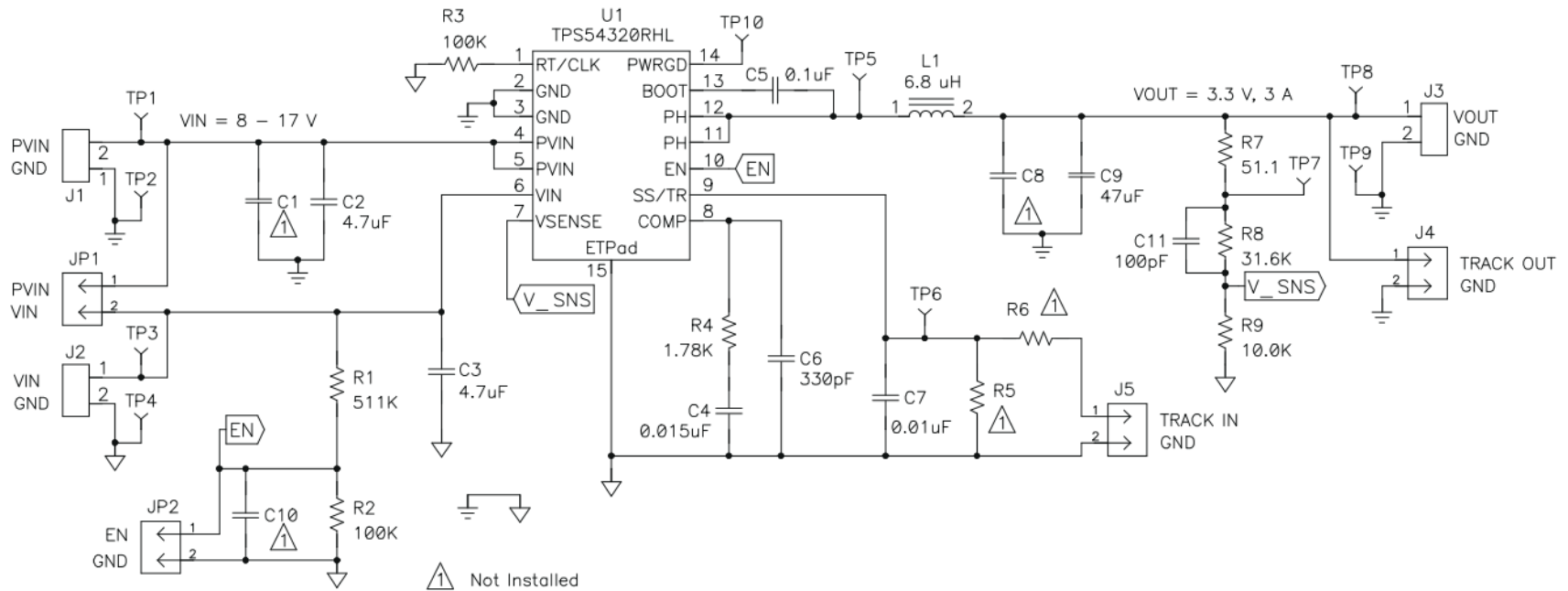
- Select a point in the feedback loop where the loop is confined to a single path
- A low impedance is driving into a high impedance

Injection Method



Loop Design Example – TPS54320

Synchronous Buck



Analyzer Setup

Analyzer Control

Turn On DC voltage

Take Data at Start Freq. Run Sweep

Start Freq (Hz) 10

Stop Freq (Hz) 480 k

Log Sweep Steps/Decade 10

AC Volts Out (VAC peak): 40 m

DC Volts Out (VDC): 0

Waveform Sine

Output Imp (Ohm): 50

Servo Control

☐ Servo On: CH1

AC Volts In (Vrms): 20 m

AC Out Step Size (dB): 10

Max AC Volts Out (Vpk): 10

☐ Auto disable servo when gain get close 0dB.

☐ Auto enable servo for frequency range:

Servo Start Freq (Hz) 10

Servp Stop Freq (Hz) 480 k

Integration

Time (sec) 1

Delay: 0

Input Imp (Ohm): 1e6

Maximum Change Between Data Points

☐ Gain (dB): 10

☐ Phase (Deg): 20

Option

☐ 350b operating Mode ☐ Sync Output

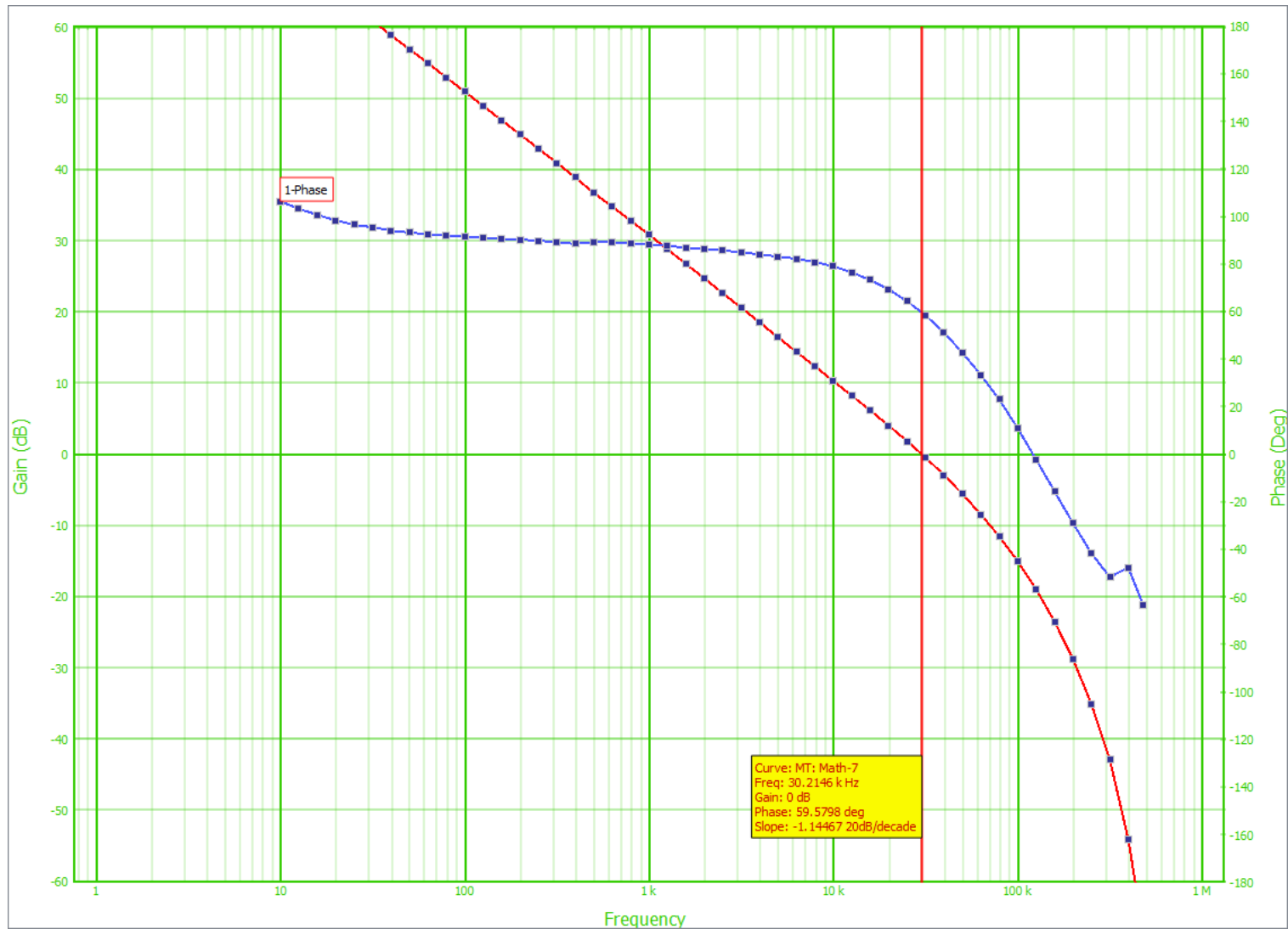
☐ High Noise Algorithm ☐ Digital Interface

Circuit Under Test: DC

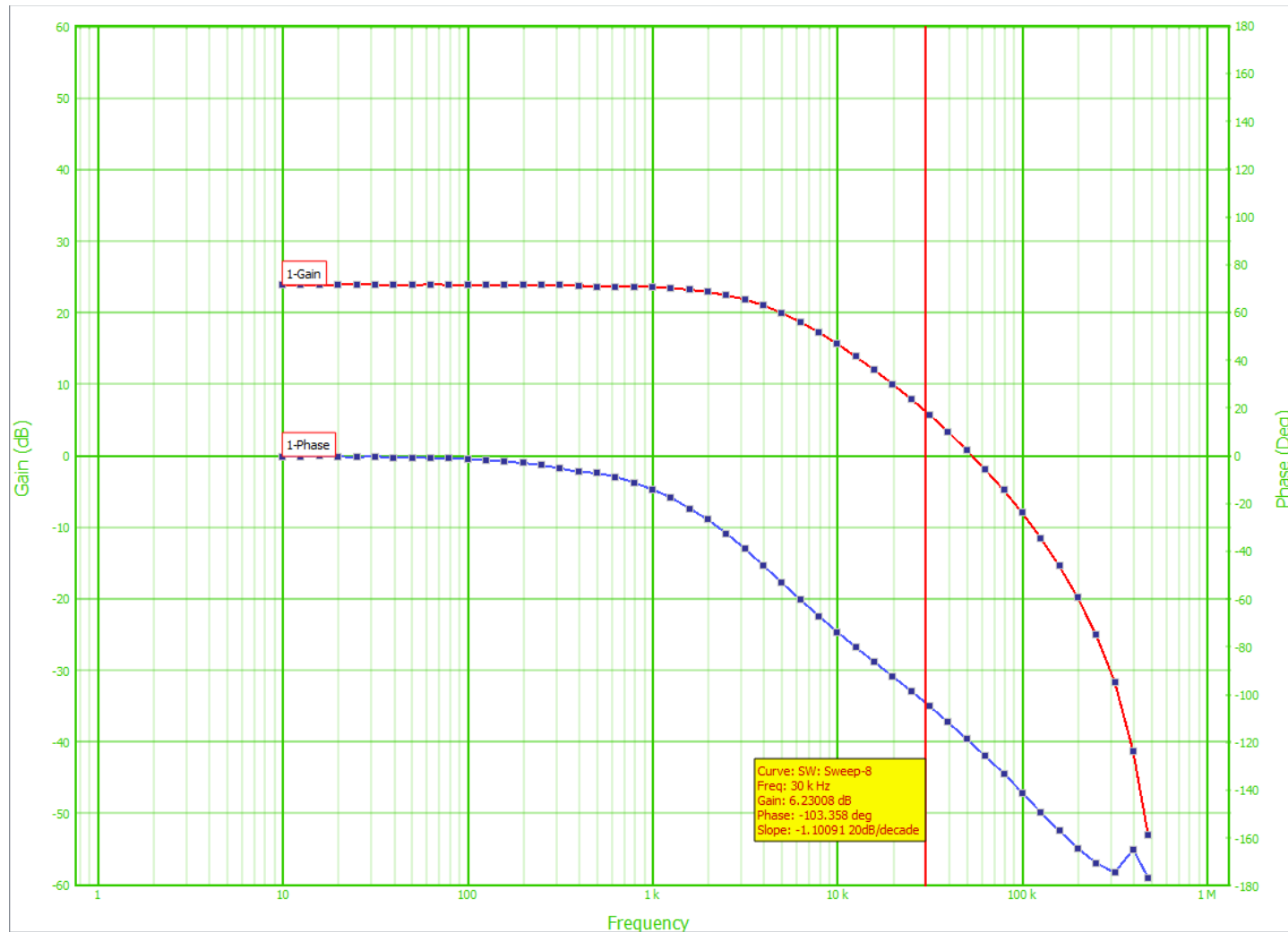
Manual Channel Ranging

CH1 AUTO CH2 AUTO

Loop Gain Bode Plot



Modulator (Control-to-Output) Bode Plot



HOW TO COMPENSATE A LOOP

- Measure/model the control-to-output transfer function.

$$G(s)$$

- Decide on an overall loop bandwidth and phase margin.

$$F_c = 30 \text{ kHz}, \quad \Phi_m = 60^\circ$$

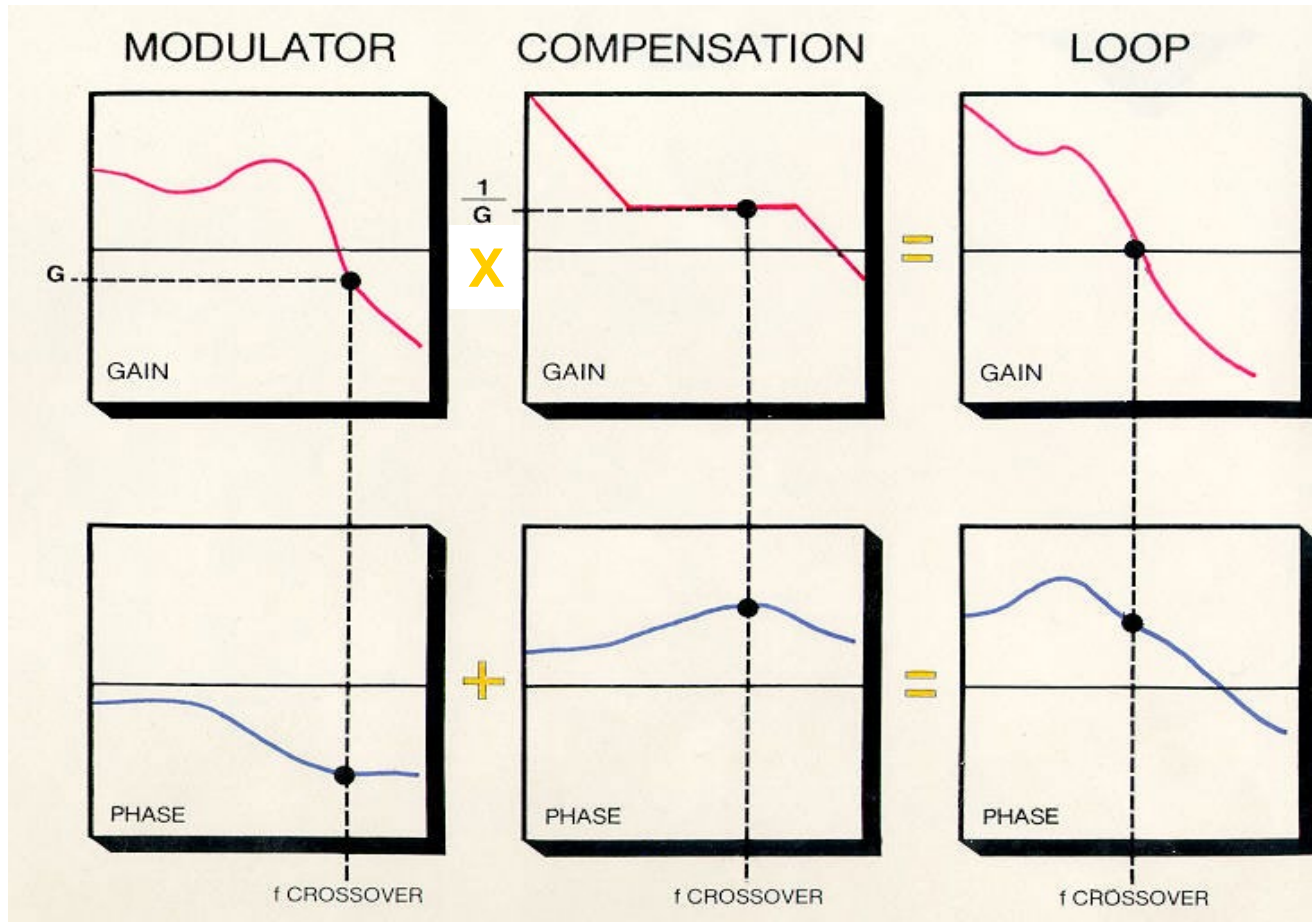
- Design the error amplifier gain at crossover, f_c .

$$G_c = 6.23008 \text{ dB}, \quad H_c = 1/G_c = -6.23008 \text{ dB} = 0.4881$$

- Design the error amplifier phase boost at f_c .

$$\text{Boost} = \Phi_m - \Phi(G_c) - 90^\circ, \quad \Phi(G_c) = -103.36^\circ$$

$$\text{Boost} = 73.36^\circ$$



Circuit Analysis and Synthesis Menu

venable6

Loop Design | Component Values | Circuit (CKT) Model | Circuit Analysis | Frequency (AC) Analysis

default.DES

Open Design File Save Design File Compute Component Values

Design files (*.DES) capture all loop design parameters and current component values

Overall Loop Circuit		Control-to-Output (or Modulator) Circuit	
Crossover Frequency	30 k Hz	Gain at Crossover Frequency	6.23008 dB
Desired Phase Margin	60 degree	Phase at Crossover Frequency	-103.358 degree

Error Amplifier Circuit

Maximum circuit complexity	2	1, 2 or 3
<input checked="" type="checkbox"/> Circuit is Inverting		
Amplifier Topology	Transconductance	
Input Resistor (R1)	10 k	Ohms
Input Voltage	3.3	VDC
Reference Voltage	800 m	VDC
Common Mode Voltage	800 m	VDC

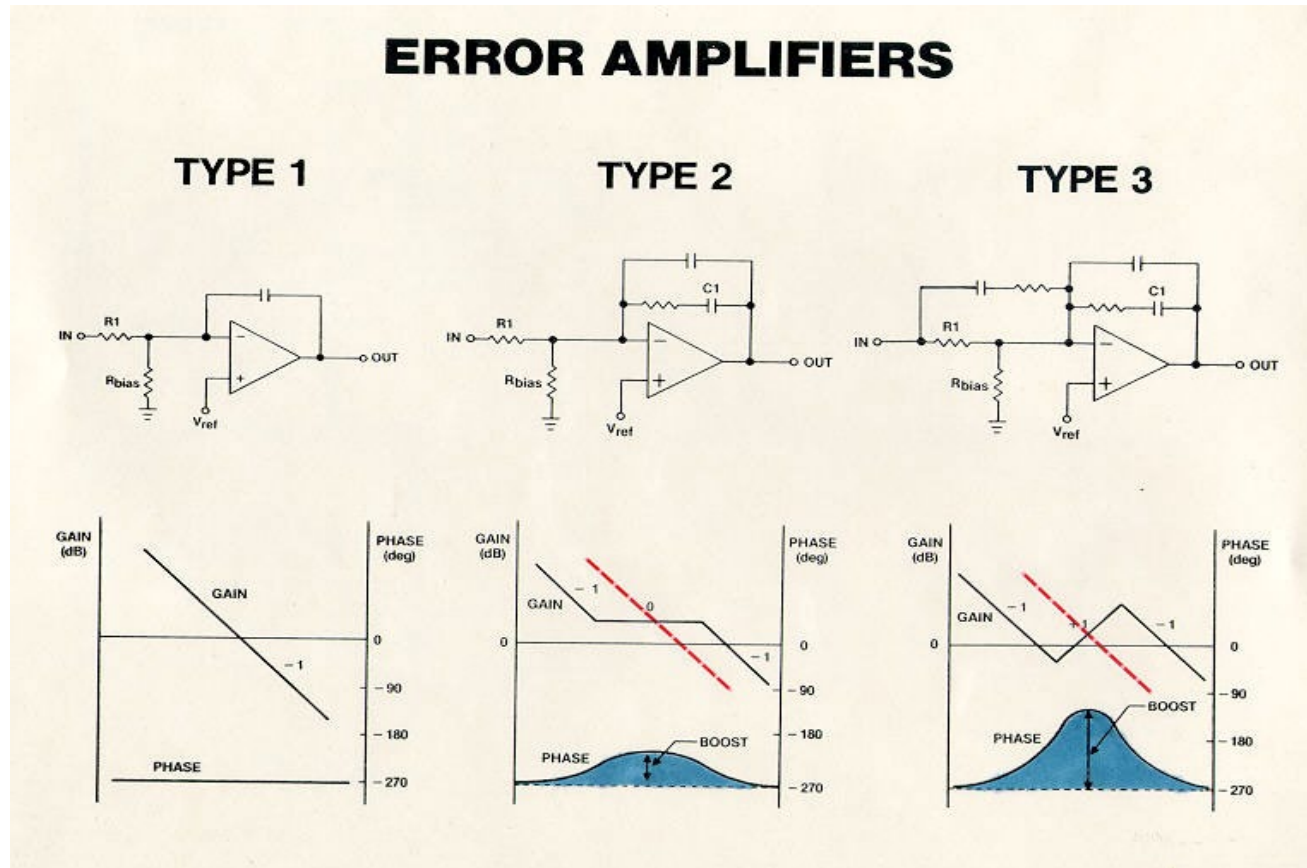
Op Amp Selection

default.AMP

Open Op Amp File Save Op Amp File

Bandwidth	10 M	Hz
Gain	69.8	dB
Transconductance	1.3 m	Mhos
Internal R	2.37715 M	Ohms

Choose an Amplifier Topology :



Error Amplifier Topology

Error Amplifier Circuit

Maximum circuit complexity

2

1,2 or 3

☒ Circuit is Inverting

Amplifier Topology

Transconductance

Input Resistor (R1)

10 k

Ohms

Input Voltage

3.3

VDC

Reference Voltage

800 m

VDC

Common Mode Voltage

800 m

VDC

Op Amp Selection

default.AMP

Open Op Amp File

Save Op Amp File

Bandwidth

10 M

Hz

Gain

69.8

dB

Transconductance

1.3 m

Mhos

Internal R

2.37715 M

Ohms

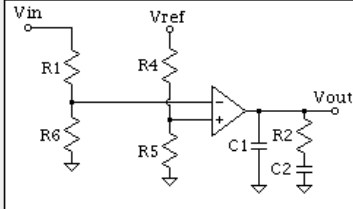
Error Amplifier Component Values

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Loop Design Component Values Circuit (CKT) Model Circuit Analysis Frequency (AC) Analysis

Print Schematic Make CKT model from component values

R1	10 k	Ohms	C1	470 p	F
R2	1.58 k	Ohms	C2	22 n	F
R3	0	Ohms	C3	0	F
R4	2.43 k	Ohms	C4		F
R5	1E21 (Big)	Ohms			
R6	3.24 k	Ohms			



☒ Automatically round off component values when they are calculated

Round off component values

Resistor Tolerance 1%

Capacitor Tolerance 10%

Phase boost 73.3581 Deg First zero at 4.57868 k Hz

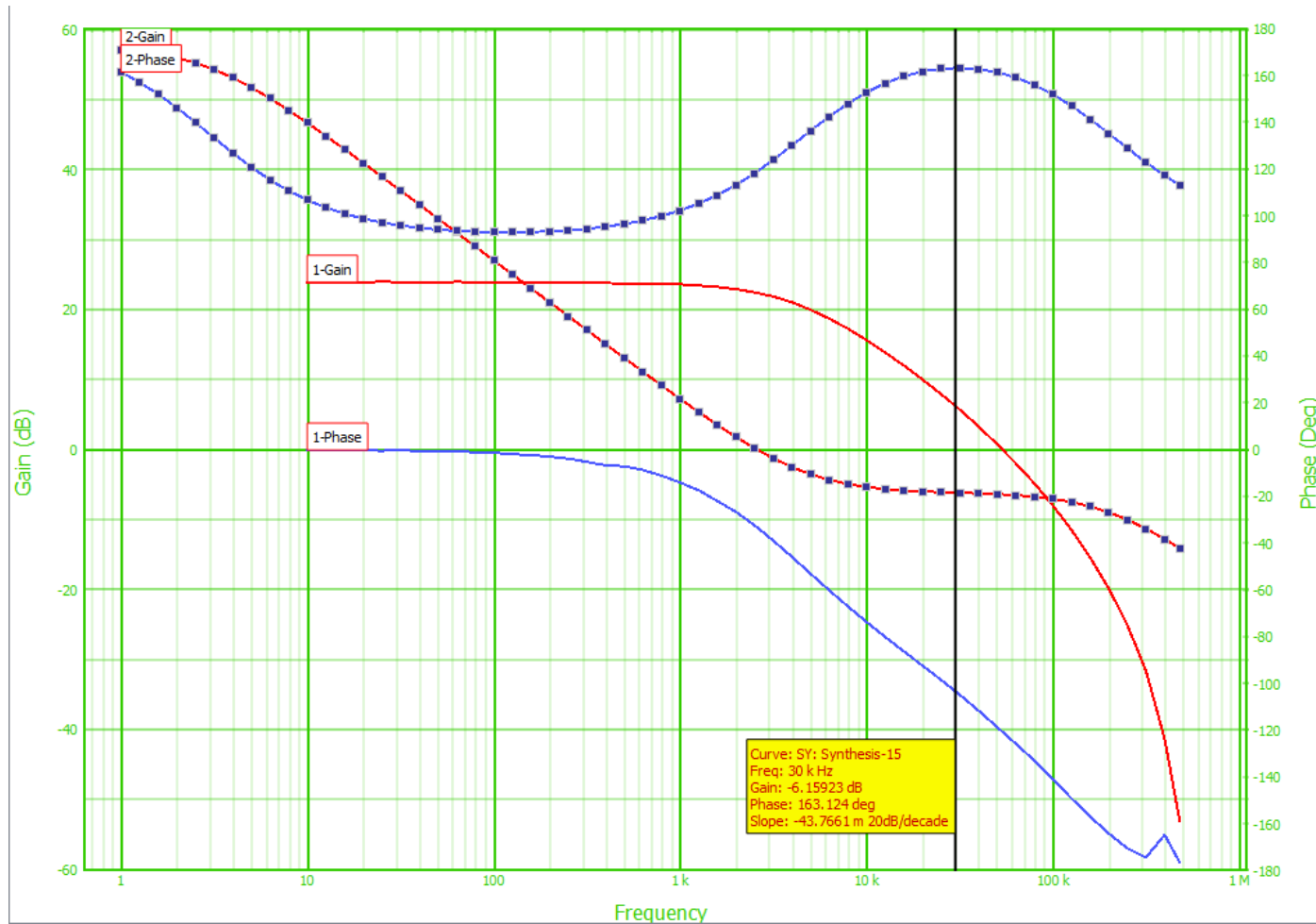
Actual phase margin 60 Deg Second zero at 0 Hz

Figure of merit 708.3 Hz First pole at 209.863 k Hz

Second pole at 0 Hz

Error Message:

Synthesized Error Amplifier Transfer Function



Multiply Modulator by Error Amp Response

Math Options for Gain-Phase Data ✕

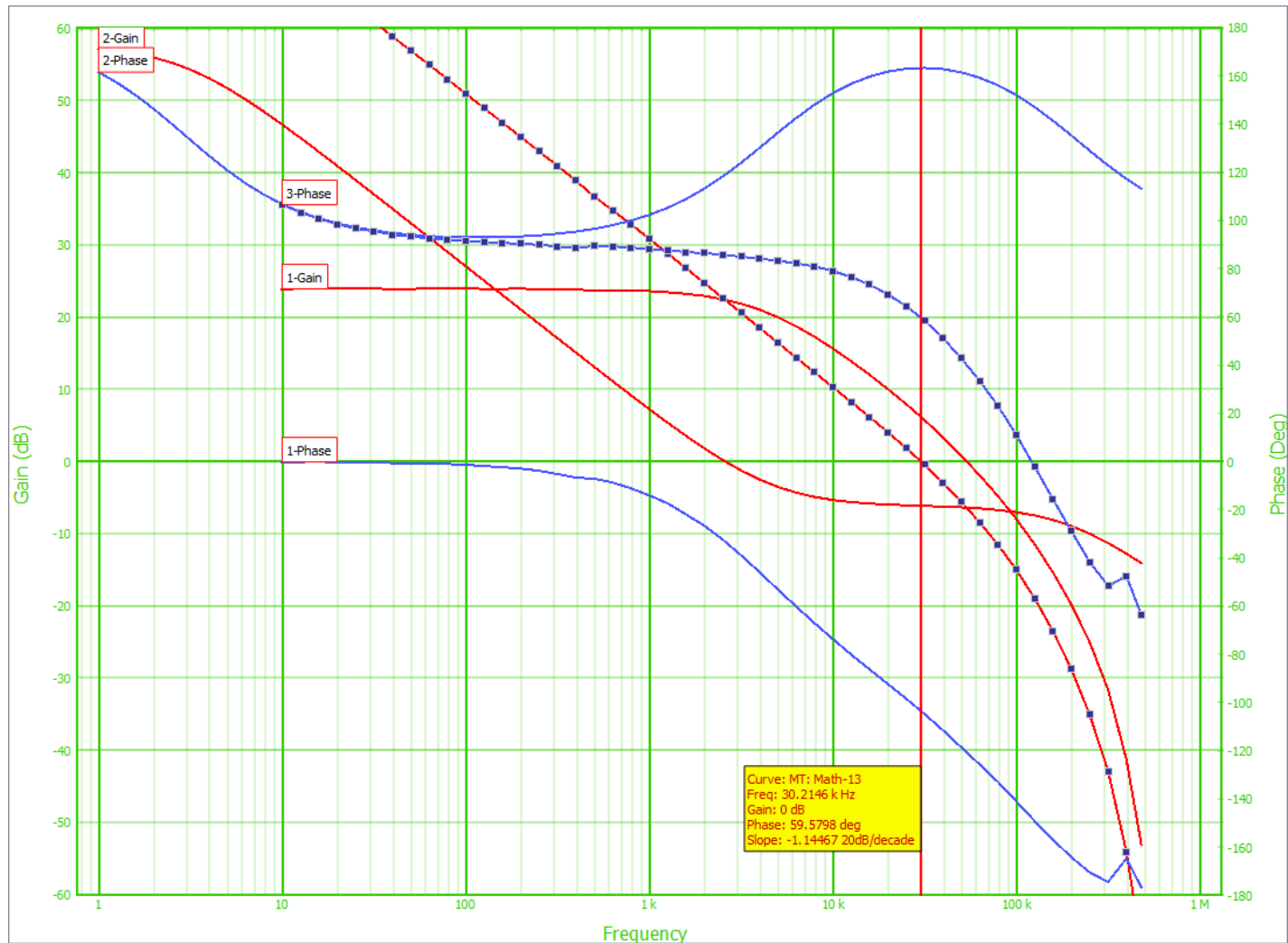
Left Operand		Right Operand	
<input checked="" type="radio"/> Data Set	1-SW: Swi ▼	<input checked="" type="radio"/> Data Set	2-SY: Syni ▼
<input type="radio"/> Scalar	1	<input type="radio"/> Scalar	1

Action

Multiply ▼

Plot

Predicted and Measured Loop Gain and Phase





Questions?

Thank You

Michael Gray, Sr. Staff Engineer

For more information on any Venable Frequency Response Analysis System, call 512-949-3144, or email info@venableinstruments.com